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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.	
09/583,233	05/31/2000	Tomomi Furudate	P108397-00011	3618	
75	90 11/19/2003	EXAMINER			
Arent Fox Kintner Plotkin & Kahn PLLC 1050 Connecticut Avenue N W Suite 600 Washington, DC 20036			HO, THANG H		
			ART UNIT	PAPER NUMBER	
		•	2188	1	
			DATE MAILED: 11/19/2003	, 6	

Please find below and/or attached an Office communication concerning this application or proceeding.

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		Application No.		Applicant(s)	K				
Office Action Summary		09/583,233		FURUDATE ET AL.	\sim_{ℓ}				
		Examiner		Art Unit					
		Thang H Ho	_	2188					
Period fo	The MAILING DATE of this communication app or Reply	ears on the cover	sheet with the c	orrespondence addre	SS				
THE I - External after - If the - If NC - Failu - Any r	ORTENED STATUTORY PERIOD FOR REPLY MAILING DATE OF THIS COMMUNICATION. Insions of time may be available under the provisions of 37 CFR 1.13 SIX (6) MONTHS from the mailing date of this communication. In period for reply specified above is less than thirty (30) days, a reply of period for reply is specified above, the maximum statutory period were to reply within the set or extended period for reply will, by statute, eply received by the Office later than three months after the mailing and patent term adjustment. See 37 CFR 1.704(b).	36(a). In no event, however within the statutory mining will apply and will expire Society cause the application to	ver, may a reply be tim num of thirty (30) days IX (6) MONTHS from become ABANDONEI	ely filed s will be considered timely. the mailing date of this community (35 U.S.C. § 133).	unication.				
1)🖂	Responsive to communication(s) filed on 09 C	October 2003 .							
2a)⊠	∑ This action is FINAL. 2b) This action is non-final.								
3)	closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11, 453 O.G. 213.								
·	on of Claims								
•	Claim(s) <u>1-7 and 9-12</u> is/are pending in the application.								
	4a) Of the above claim(s) is/are withdrawn from consideration.								
· <u> </u>	Claim(s) is/are allowed.								
·	Claim(s) 1-7 and 9-12 is/are rejected.								
· <u> </u>	Claim(s) is/are objected to. Claim(s) are subject to restriction and/or election requirement.								
	on Papers	election requirem	ient.						
· · ·	The specification is objected to by the Examiner	·.							
10) 🗆	· The drawing(s) filed on is/are: a)□ accep	oted or b) objecte	d to by the Exar	niner.					
	Applicant may not request that any objection to the	e drawing(s) be held	in abeyance. Se	ee 37 CFR 1.85(a).					
11) 🔲 -	The proposed drawing correction filed on	is: a) approve	d b)□ disappro	ved by the Examiner.					
	If approved, corrected drawings are required in rep	oly to this Office acti	on.						
12) 🗌 -	The oath or declaration is objected to by the Exa	aminer.							
Priority u	ınder 35 U.S.C. §§ 119 and 120								
13)	Acknowledgment is made of a claim for foreign	priority under 35	U.S.C. § 119(a))-(d) or (f).					
a)[☐ All b)☐ Some * c)☐ None of:								
	1. Certified copies of the priority documents have been received.								
	2. Certified copies of the priority documents have been received in Application No								
* S	3. Copies of the certified copies of the prior application from the International Bursee the attached detailed Office action for a list of the control of th	reau (PCT Rule 1	7.2(a)).		ge				
14) 🗌 A	cknowledgment is made of a claim for domestic	c priority under 35	U.S.C. § 119(e) (to a provisional ap	olication).				
) The translation of the foreign language pro Acknowledgment is made of a claim for domesti	• •							
Attachmen	t(s)		-						
2) Notic	e of References Cited (PTO-892) e of Draftsperson's Patent Drawing Review (PTO-948) nation Disclosure Statement(s) (PTO-1449) Paper No(s)	5) 🗌	Notice of Informal F	(PTO-413) Paper No(s) atent Application (PTO-15					

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DETAILED ACTION

Response to Amendment

- 1. This Office Action is in response to applicants' amendment dated 10/09/2003. The applicant's remarks and amendment were considered with the results that follow.
- 2. Claims 1-12 are pending in this application for examination. Claims 1, 7, 9 and 10 have been amended, claim 8 has been cancelled and claims 11-12 have been added. Therefore, claims 1-7 and 9-12 remain pending in the application.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

- (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
- 4. Claims 5-7 and 10 are rejected under 35 U.S.C. 102(b) as being anticipated by Imura et al. (USPN 5,398,212).

As per claim 5, Imura discloses in figure 1 a semiconductor memory device comprising a plurality of memory cells (3), an invalid address detecting circuit (5) for detecting address signal supplied from exterior indicating an address space other than the address space, and an output controlling circuit (6) which can be programmed to output, when the invalid address detecting circuit carries out detection in a read operation, a data

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signal read in a read operation cycle immediately preceding a read operation (e.g. see column 6, lines 52-54).

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As per claim 6, Imura further discloses in figure 5 an output circuit for receiving a read data signal from memory cells (3) and continuously outputting the received data to the exterior, according to a control by the output controlling circuit (6) when the invalid address detecting circuit carries out detection in the read operation.

Claim Rejections - 35 USC § 103

- 5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:
 - (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
- 6. Claims 1-4 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Imura et al. (USPN: 5,398,212), hereinafter Imura; in view of Howard (USPN: 5,754,816).

As per claim 1, Imura disclose the device as claimed including a semiconductor memory device in FIG. 1 comprising: a plurality of memory cells (3) corresponding to an address space larger than 2ⁿ and smaller than 2⁽ⁿ⁺¹⁾, where n is a positive integer; and an invalid address detecting circuit (5) for detecting that an address signal supplied from exterior indicates an address space other than the address space (e.g. column 5, lines 31 through column 6, lines 11).

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Imura does not disclose expressly the invalid signal outputting circuit for outputting an invalid signal to the exterior of the semiconductor memory device when the invalid address detecting circuit carries out the detection, thereby notifying a system unit accessing the semiconductor memory device of the detection.

Howard teaches in FIG. 1 the concept of memory access and controls, specifically the usage of an invalid signal outputting circuit (12) for outputting an invalid signal to notify the system of the detection and to prevent further processing. Howard teaches that the usage of an invalid access signal would not only provide feedback status of the memory access operation to the requesting unit, but also the additional power savings resulting from the elimination of further processing including address decoding and data outputting from the requested memory location are not needed (e.g. see figure 2, and column 4, lines 7-20). Imura and Howard are analogous art because they are from the same field of endeavor in memory accessing and control.

It would have been prima facie obvious for one skilled in the art at the time the invention was made to implement a semiconductor memory device as taught by Imura and modify the device to include an invalid signal outputting circuit as taught by Howard to generate the claimed invention with a reasonable expectation of success.

One skilled in the art would have been motivated to do so because it would reduce power consumption by only access valid memory location preventing invalid address from propagating to the output circuit and to provide the status of the memory access to the requesting unit preventing invalid data from being process that could put the system in unpredictable state.

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As per claim 2, Imura discloses that the device further comprising an output controlling circuit (7) for outputting, when the invalid address detecting circuit (5) carries out the detection in a read operation, a data signal read in a read operation cycle immediately preceding the read operation (i.e. before the data being outputted from the output buffer circuit (4)).

As per claim 3, Imura discloses in figure 6 the device further comprising an output circuit (4) for receiving a read data signal from the memory cells (3) and continuously outputting the received data to the exterior, according to a control by the output controlling circuit (7) when the invalid address detecting circuit carries out the detection in the read operation.

As per claim 4, Imura discloses the outputting of high impedance when the invalid address detecting circuit detects an invalid address in a read operation (e.g. see table 2, column 8, lines 57 et seq.).

As per claim 7, the combination of Imura and Howard discloses the semiconductor memory device substantially as claimed including the usage of a flash memory device (column 5, lines 17-22) and a command controlling circuit for validating the command input indicating the address space other than the address space. Imura does not disclose expressly the command controlling circuit for accepting and validating

command control inputs specifically neither in controlling a write nor an erase operation. However, it is well known in the art of flash memory that a flash memory device is an electrically write-able and erasable device and it is capable of accepting a write and erase command. It is inherent that, in order to implement the semiconductor memory device utilizing flash memory, the command control circuit would need to be modified or reprogrammed to carry out a write and erase operation.

As per claim 10, it encompass the same scope of invention as to that of claim 7 above, however it is drafted as method format rather than apparatus format, the claim is therefore rejected for the same reasons as being set forth above.

As per claim 9, it encompass the same scope of invention as to that of claims 1-4 above, however it is drafted as method format rather than apparatus format, the claim is therefore rejected for the same reasons as being set forth above.

As per claim 11, the combination of Imura and Howard disclose a semiconductor memory device further comprising a decoder, which decodes the address signal, and is inactivated when the invalid address detecting circuit carries out the detection (e.g. Imura, FIG. 5, element 2 including an invalid access signal as taught by Howard for controlling the address decoder (2)).

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As per claim 12, the combination of Imura and Howard discloses a sense amplifier which amplifies a data signal read from the memory cells, and is inactivated when said invalid address detecting circuit carries out the detection (e.g. Imura, column

5, lines 57-58).

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Response to Arguments

7. Applicants' arguments filed 10/09/03 with respect to Claims 1-4, 7, 9-12 are moot in view of the new ground(s) of rejection.

8. Applicants' arguments filed 10/09/03 with respect to Claim 5 have been fully considered but they are not persuasive.

Applicants asserted:

- (a) Imura fails to disclose or suggest at least the limitation of "an output controlling circuit for outputting, when said invalid address detecting circuit carries out said detection in a read operation, a data signal read in a read operation cycle immediately preceding said read operation".
- (b) Imura merely shows a non-empty address is accessed after detecting an empty address... present invention provides that a read operation is not carried out when an address is detected as an empty address... provides that the read data, having been accessed and read in advance.
- (c) Semiconductor memory device of the present invention is neither comparable nor analogous to that which is shown in Imura... Imura requires a circuit for converting the received empty address into non-empty address...

Examiner respectfully traverses Applicants' remark for the following reasons:

With respect to (a), Imura does teach an output controlling circuit for outputting, when said invalid address detecting circuit carries out said detection in a read operation, a read data signal read in a read operation cycle immediately preceding said read operation. FIG. 1 shows a programmable output controlling circuit (6) that can be programmed to

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output or inhibit the data from being output upon detection of an invalid address in a read operation cycle immediately preceding said read operation (i.e. before the data being outputted from the output buffer circuit (4) (e.g. column 6, lines 33-37 and column 6, lines 52-54).

With respect to (b), the argument is not persuasive because it is not commensurate in scope with the claim. Claim 5 contains neither the limitation of not carrying out the read operation nor providing of the read data, having read in advance.

With respect to (c), first of all, Imura's invention and the present invention are both directed to the same field of endeavor (memory accessing and control) of a semiconductor memory device specifically the detection of an invalid address and controlling the outputting of the data. Secondly, Claim 5 does not require the exclusion of a conversion circuit. Thus, the two inventions are comparable and analogous.

Therefore, the rejection of claims 5-6 is deemed to be proper. Imura discloses each and every element recited within claims 5-6.

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Conclusion

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9. THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thang H Ho whose telephone number is 703-305-1888. The examiner can normally be reached on Monday-Friday from 7:00 A.M. - 4:30 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on 703-306-2903. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-9600.

Thang Ho Art Unit 2188 November 13, 2003

Kevin L. Ellis Primary Examiner

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